CHUKA  **UNIVERSITY**

UNIVERSITY EXAMINATIONS

EXAMINATION FOR THE AWARD OF DEGREE OF BACHELOR OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING

EENG 394: DIGITAL ELECTRONICS

STREAMS: **TIME:2 HOURS**

DAY/DATE: THURSDAY 13/04/2023 **8.30 A.M. –10.30 A.M.**

INSTRUCTIONS

Answer question ONE and any other TWO questions
Do not write on the question paper

QUESTION ONE

a. Differentiate between combinational and sequential circuits (2 Marks)

b. Define the following terms as used in digital electronics (4 Marks)

   i. Canonical form
   ii. Logic gates
   iii. Flip-flop
   iv. Karnaugh map

c. How do you implement three-input and four-input EX-OR logic functions with the help of two-input EX-OR gates? (3 Marks)

d. Convert the decimal number 2497.50_{10} to its equivalent octal (4 Marks).

e. Typically, digital thermometers use BCD to drive their digital displays (3 Marks).

   i. How many BCD bits are required to drive a 3-digit thermometer display?
   ii. What 12-bits are sent to display for a temperature of 157 ºC?

f. Use a Karnaugh map to minimize the following POS expression (4 Marks)

$$(B + C + D)(A + B + \overline{C} + D)(\overline{A} + B + C + \overline{D})(A + \overline{B} + C + D)(\overline{A} + \overline{B} + C + D)$$

g. Minimize the following function and realize the minimized function using NOR gates (4 Marks)

$$F(A, B, C, D) = B\overline{C} + \overline{A}\,B + BC\overline{D} + \overline{AB}D + A\overline{BC}D$$

h. Simplify the following expression using De Morgan's theorems [3 Marks].

$$\overline{A\ \overline{(B + \overline{C})}\ D}$$

i. Minimize the given Boolean expression using K-map (3 Marks).

$$F(A, B, C, D) = \sum m\,(3, 4, 5, 7, 9, 13, 15)$$

QUESTION TWO

a. i. Explain three characteristics of CMOS logic circuit (3 Marks)?

ii. Explain the operation of a CMOS NAND gate (4 Marks)

b. A binary counter is being pulsed by a 512 kHz clock signal. The output frequency from the last flip-flop is 4 kHz. Determine

i. the MOD number and (2 Marks)

ii. the counting range (2 Marks).

c. An electrical control system uses three positional sensing devices, each of which produce 1 output when the position is confirmed. These devices are to be used in conjunction with a logic network of AND and OR gates and the output of the network is to be 1 when two or more of the sensing devices are producing signals of 1. Draw a network diagram of a suitable gate arrangement. (5 Marks)

d. Design a combinational logic circuit for the given Boolean function using a Decoder (4 Marks)

$$Y = A.\overline{B}.\overline{C} + \overline{A}.B.\overline{C} + A.B.C + \overline{A}.\overline{B}.\overline{C}$$

QUESTION THREE

a. i. Explain the difference between multiplexer and demultiplexer (1 Mark)?

ii.Describe the operation of a 8 to 1 multiplexer (4 Marks).

iii. An Engineer require a binary ripple counter that counts 000 and 111 and skips the remaining six states, that is, 001, 010, 011, 100, 101 and 110. Using a presentable,

clearable negative edge-triggered J-K flip-flops with active LOW PRESET and CLEAR inputs,

i. Design a binary ripple counter (3 Marks)

ii. Draw the timing waveforms (2 Marks)

iii. Determine the frequency of different flip-flop outputs for a given clock frequency, f (1 Mark)

iv. Using a K-map simplify the following function and realize using NAND gate (6 Marks)

$$F(A, B, C, D) = \sum(1, 4, 6, 7, 8, 9, 10, 11, 15)$$

v. Explain three uses of Counters in digital systems (3 Marks)

QUESTION FOUR

a. Design a full adder circuit from half adders starting with a truth table and the resulting equations (10 Marks).

b. Draw the circuit of gates that would effect the function

$$F = \overline{A + B.C}$$

Simplify this function and hence redraw the circuit that could effect it (6 Marks)

c. Compare and contrast the differences between analog and digital signals (4 Marks)
