CHUKA  **UNIVERSITY**

UNIVERSITY EXAMINATIONS

EXAMINATION FOR THE AWARD OF BACHELOR OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING

EENG 476: MICROPROCESSORS II

STREAMS: BSc. EENG **TIME: 2 HOURS**

DAY/DATE: TUESDAY 19/12/2023 **8.30 A.M. – 10.30 A.M.**

INSTRUCTIONS

- **Answer question ONE and any other TWO questions**
- **Do not write on the question paper**

QUESTION ONE (30 MARKS)

a) What is the stack memory? (2 marks)

b) We use two main instructions to control the movement of data into a stack and from a stack. Briefly discuss. (4 marks)

c) What is a Subroutine in assembly language? (2 marks)

d) Draw the 8085 microprocessor and classify the pins accordingly. (5 marks)

e) Briefly illustrate how parallel and serial buses work. (4 marks)

f) Use a diagram to illustrate the bus structure of the 8085. (4 marks)

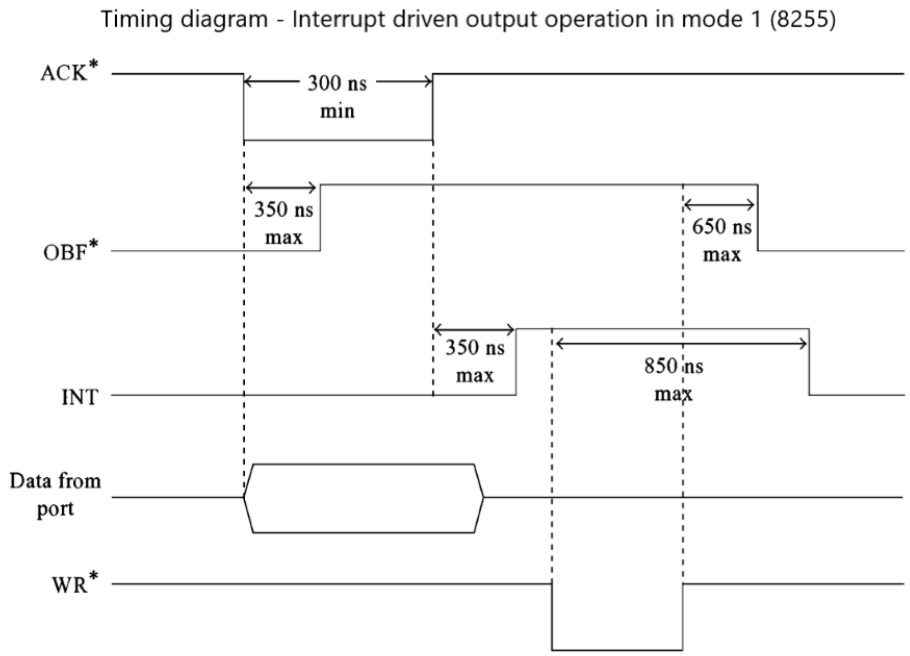
g) The Intel 8085 are five distinct interrupt pins which are used as the Hardware Interrupts list any four. (2 marks)

h) Explain the working of vectored interrupts. (4 marks)

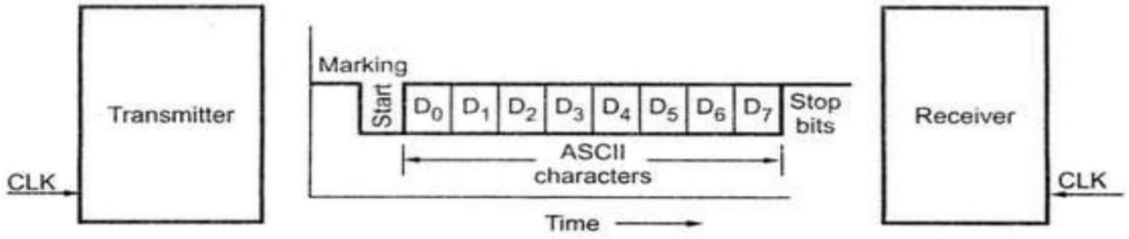
i) Discuss the Asynchronous Serial Data Transfer. (3 marks)

Question Two (20 marks)

a) The diagram below shows an interrupt driven timing diagram for an 8255 PPI. Discuss the steps. **(6 marks)**

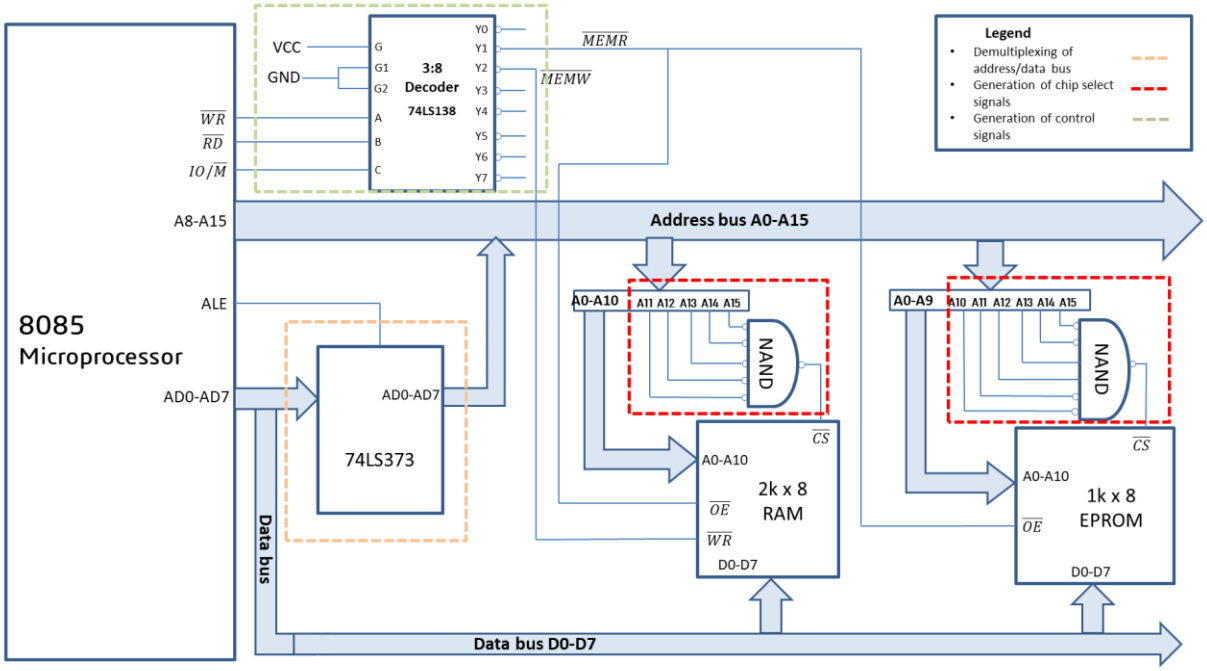


b) Discuss the Asynchronous Serial Data Transfer at the transmitter and receiver end. (**6 marks)**



c) Use diagrams to distinguish Memory-Mapped I/O Interfacing and Isolated I/O interfacing (4 marks)

d) The diagram below summarizes the entire process of interfacing the external memory with the 8085 microprocessor. Briefly discuss the significance of the pins involved. (4 marks)



Question Three (20 marks)

a) Why can't we perform arithmetic or logical operations on I/O data in I/O mapped I/O mode? (4 marks)

b) Serial data communication can be categorized on the basis of how data transmission occurs as simplex, half duplex and full duplex. Explain the significance of these terms. (3 marks)

c) Discuss the Device/Direct Memory Access (DMA) Data Transfer method using a diagram. (8 marks)

d) What is the significance of the code below? (5 marks)

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LXI H, 8000H
SPHL
LXI H, 1234H
PUSH H
POP D
HLT
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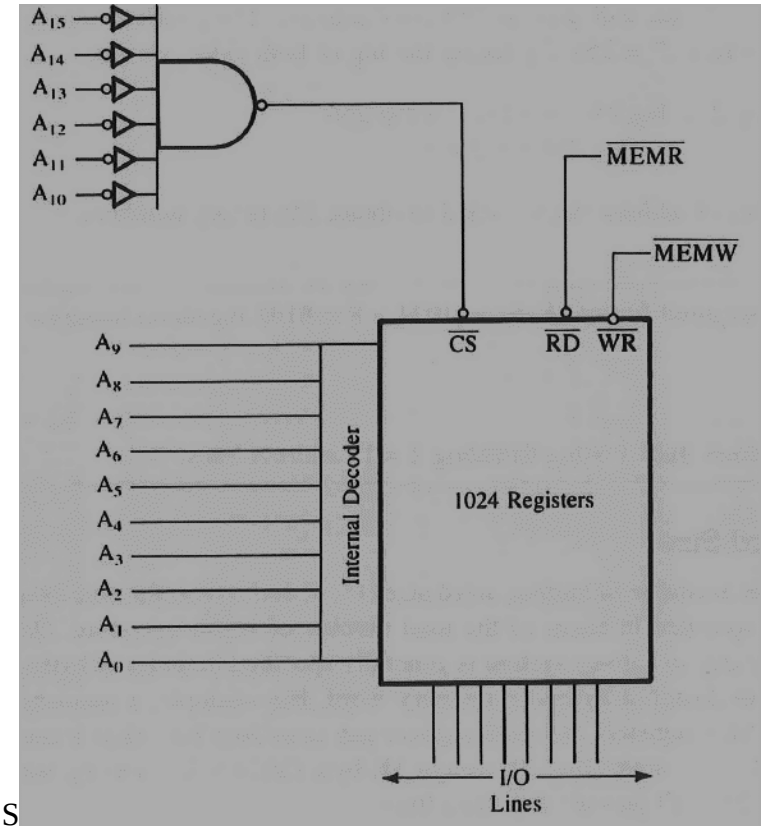
Question Four (20 marks)

a) Suppose we have the instruction STA 2050H to store the content of the accumulator to the memory address provided. Calculate the number of T-states. (5 marks)

b) Draw and explain the timing diagram of an Opcode fetch machine cycle. (10 marks)

c) Explain the memory address range of 1K (1024x8) memory shown in the figure below and explain the changes in the addresses if the hardware of the $\overline{CS}$ line is modified.

(5 marks)



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