CHUKA UNIVERSITY

UNIVERSITY EXAMINATIONS

THIRD YEAR EXAMINATION FOR THE AWARD OF DEGREE OF BACHELOR OF SCIENCE IN COMPUTER SCIENCE

COMP 304: COMPONENTS AND DESIGN TECHNIQUES FOR DIGITAL SYSTEMS

STREAMS: **TIME: 2 HOURS**

DAY/DATE: WEDNESDAY 6/12/2017 **8.30 A.M – 10.30 A.M**

INSTRUCTIONS:

- **Answer all questions in section A and any other two questions from section B.**
- **No Reference Material is allowed in the exam Room.**
- **All Mobile phones should be switched off in the exam room.**

SECTION A (COMPULSORY)

QUESTION 1(COMPULSORY) [30 MARKS]

a) Using a TTL diagram, explain the operation of a NAND gate. (4marks)

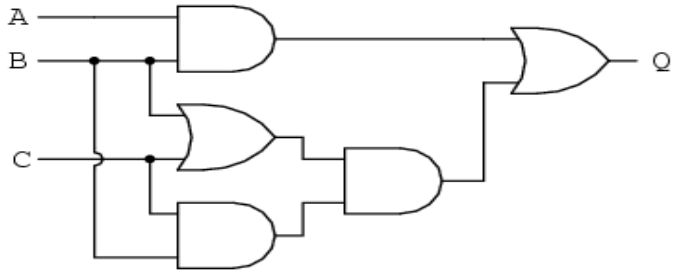
b) Using "*ieee.std_logic_1164.all"* library, write aVHDL program of a J-K flip flop. (5marks)

c) With reference to counters, answer the following questions.
   i. With the help of a digital circuit diagram, explain how a digital upwards counter functions (5marks)
   ii. Draw the FSM diagram of the digital upward counter in (i) above (3marks)

d) Use Karnaugh maps SOP to minimize the following circuit. (5 marks)

$$Z = \bar{A} + AB + A\bar{B}C + A\bar{B} + C$$

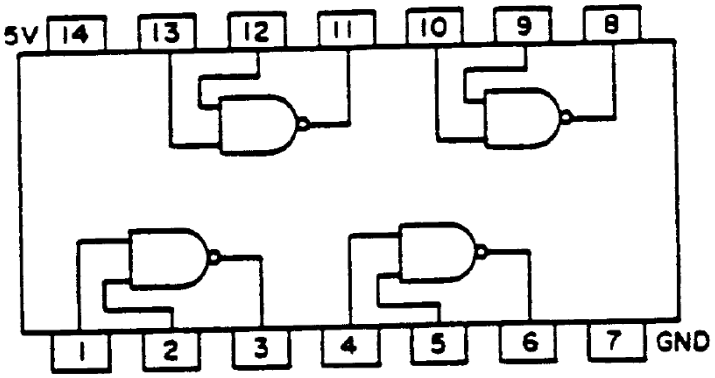
e) Below is a digital circuit. Use it to answer the questions below: -



i) Simplify the above circuit (show the simplification process) (3marks)

ii) Draw the simplified circuit using NAND gates only (2marks)

iii) With the help of a diagram, illustrate how you would implement the simplified circuit using 7400 series IC shown below (3marks)



SECTION B (Answer **two question** from this section**)**

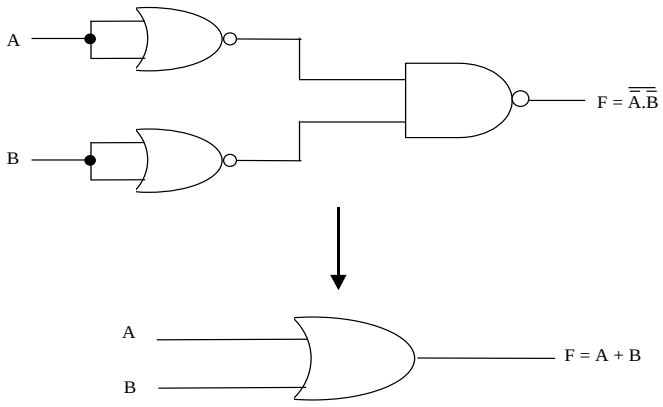
QUESTION 2 [20 MARKS]

a) A certain digital device could count number 1up to 16 in binary numbers. Draw a circuit which will enable this device give output of logic 1 only where there are three consecutive ones. i.e. 0111, 1110 etc. (9marks)

b) Use Demorgan theorem to prove that the following circuits are the same

i) A + A B = A (3marks)

ii)



(4marks)

c) With regard to the principle of universality of NOR gates, using sketch diagrams, show how NOR gates could be used as: -
   i) AND gate
   ii) NAND gate (4marks)

QUESTION 3 [20 MARKS]

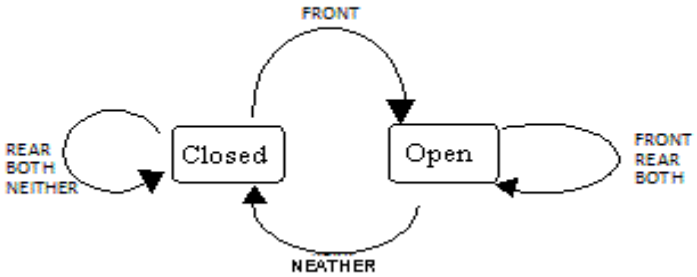
a) With reference to decoders
   i) Draw a circuit diagram of an8 to 3 encoder using INVERTERs and gates only (4marks)
   ii) Draw a truth table of the above encorder (4marks)
   iii) Using "*ieee.std_logic_1164.all"* library, write a VHDL program of the decoder. (6marks)

b) Using a diagram, explain the operation of a full adder (6marks)

QUESTION 4 [20 MARKS]

a) With the help of a digital circuit diagram, explain how a decimal to binary encoder functions (10marks)

b) Below is a simple door open and lock FSM, explain how it functions and draw its state transition table (5marks)



c) Explain the operation of an SR flip flop (5marks)

QUESTION 5 [20 MARKS]

a) A certain student was tasked with designing a full adder which follows the following states

Since the carry variable can either be 1 or 0. When the circuit is in the state where carry = 0, the relationship between the inputs A and B and the output S is such that: if AB = 00 then S = 0; if AB = 01 then S = 1; if AB = 10 then S = 1; and if AB = 11 then S = 0. When the circuit

is in the state where carry = 1, it also follows that: if AB = 00 then S = 1; if AB = 01 then S = 0; if AB = 10 then S = 0; and if AB = 11 then S = 1.

i) Draw an FSM diagram of the above scenario (6marks)
ii) Draw a state transition table of the above FSM (6 marks)

b) Using a Boolean, write an example of the following laws: -
i) Dominance (2marks)
ii) Commutative (2marks)
iii) Idempotent (2marks)
iv) involution (2marks)
