CHUKA  **UNIVERSITY**

UNIVERSITY EXAMINATIONS

EXAMINATION FOR THE AWARD OF DEGREE OF BACHELOR OF SCIENCE IN COMPUTER SCIENCE

COSC 110: COMPUTER ARCHITECTURE

STREAMS:Y1S1 **TIME: 2 HOURS**

DAY/DATE:TUEDAY 5/12/2017 **2.30 P.M – 4.30 P.M**

INSTRUCTIONS:

- **Answer Question One and any other two questions.**

Question One (30 marks)

(a) Discuss today's computer systems in relation with the earliest computer ENIAC. (3 marks)

(b) Discuss the stored-program concept in the John von Neumann computer architecture. (3 marks)

(c) Explain what an instruction set is in computer systems. (3 marks)

(d) Briefly explain the fetch-execute cycle in instruction execution. (3 marks)

(e) List three registers used in an instruction cycle, along with their purpose. (3 marks)

(f) Briefly discuss the concept of pipelining in design of computer systems. (3 marks)

(g) Explain the difference between Interrupt Driven I/O and Direct Memory Access I/O techniques. (3 marks)

(h) Explain why branch prediction will speed up the processor. (3 marks)

(i) Given a memory reference a Cache has to determine if the memory is in the Cache. There are a number of schemes for determining where a global memory reference should be placed in the cache memory. Describe the following Schemes: Direct mapped and n-way associative mapping caches. (6 points)

Question Two (20 marks)

(a) Describe the four major internal structural components of a computer system. Use a well labeled diagram to illustrate their interconnection in the von Neumann architecture. (9 marks)

(b) Assume:

- A processor has a direct mapped cache

- Data words are 8 bits long (i.e. 1 byte)
- Data addresses are to the word
- A physical address is 20 bits long
- The tag is 11 bits
- Each block holds 16 bytes of data

How many blocks are in this cache? Explain your answer. (6 marks)

(c) Explain what is a pipeline hazard? Discuss three types of pipeline hazards. (5 marks)

Question Three(20 marks)

(a) Discuss the following memory access modes. Give the memory devices involved in each case. (9 marks)

(i) Random access
(ii) Direct access
(iii) Sequential access

(b) The 5 stages of the processor have the following latencies:

	Fetch	Decode	Execute	Memory	Write back
a	300ps	400ps	350ps	550ps	100ps
b	200ps	150ps	100ps	190ps	140ps

Assume that when pipelining, each pipeline stage costs 20ps extra for the registers between pipeline stages.

(i) For non-pipelined processor, what is the cycle time? What is the latency of an instruction? What is the throughput? (5 marks)

(ii) For a pipelined processor, what is the cycle time? What is the latency of an instruction? What is the throughput? (6 marks)

Question Four(20 marks)

(a) Consider a *16-way set-associative* cache

- Data words are *64 bits* long
- Words are addressed to the *half-word*
- The cache holds 2 Mbytes of data
- Each block holds 16 data words
- Physical addresses are 64 bits long

How many bits of tag, index (set), and offset (word address) are needed to support references to this cache? (10 marks)

(b) On the instruction cycle, explain how the cycle is affected when interrupts are enabled. Discuss the expected changes in the flow of program execution. Use an appropriate diagram to illustrate your answer. (10 marks)

Question Five(20 marks)

(a) According to Flynn's classification of computer systems, there are four classifications. (12 marks)

(i) Explain the differences between SIMD and SISD processors.
(ii) Explain the basic characteristics of SIMD processors.
(iii) Give one example of a problem that can be solved effectively with an SIMD architecture processor.
(iv) Some modern high performance processors have capabilities of an SIMD machine. Explain this statement.

(b) Describe the following cache write policies. (8 marks)

(i) write-through
(ii) write-back
