CHUKA  **UNIVERSITY**

UNIVERSITY EXAMINATIONS

EXAMINATION FOR THE AWARD OF DEGREE OF BACHELOR OF SCIENCE IN COMPUTER SCIENCE

COSC 110: COMPUTER ARCHITECTURE

STREAMS: Y1S1 **TIME:2 HOURS**

DAY/DATE:MONDAY 2/12/2019 **8.30 A.M – 10.30 A.M**

INSTRUCTIONS:

Instruction: *Answer question one and any other two questions.*

QUESTION ONE (30 MARKS)

(a) Using an example, explain the difference between little endian and big endian byte ordering. (2 marks)

(b) Discuss four major achievements in the evolution of computer systems in relation with the today's modern computer. (4 marks)

(c) Discuss the stored-program concept in the John von Neumann computer architecture. (4 marks)

(d) Distinguish between direct mapping and 4-way set associative mapping schemes when mapping a main memory reference into the cache. (4 points)

(e) Briefly explain the fetch-execute cycle in instruction execution. (4 marks)

(f) Discuss four differences between main memory and secondary memory in computer system. (4 marks)

(g) Given a two address ISA, generate the assembly code instruction for the infix expression: `x = a + d / c * d` (4 marks)

(h) Explain the differences between programmed I/O and Interrupt Driven I/O techniques. (4 marks)

QUESTION TWO (20 MARKS)

(a) List four registers used in an instruction cycle, along with their purpose. (4 marks)

(b) On the instruction cycle, discuss how the instruction cycle and the general flow of program execution is affected when interrupts are enabled. (6 marks)

(c) Consider a *8-way set-associative* cache

- Data words are *32 bits* long; Words are addressed to the *half-word;* The cache holds 2 Mbytes of data; Each block holds 8 data words; Physical addresses are 32 bits long

How many bits of tag, index, and offset are needed to support references to this cache? (10 marks)

QUESTION THREE (20 MARKS)

(a) Briefly discuss the concept of pipelining in design of computer systems. (4 marks)

(b) Consider the infix expression x = `B + C * D - E + A`

i). write the postfix format on the instruction (2 marks)
ii). Write the stack ISA instructions for the postfix expression (7 marks)
iii). Write the one-address ISA instructions of the infix expression (7 marks)

QUESTION FOUR (20 MARKS)

(a) Explain why branch prediction will speed up the processor. (4 marks)

(b) Describe the following cache write policies. (6 marks)

(i) write-through
(ii) write-back

(c) Let the address stored in the program counter be designated by the symbol X1. The instruction stored in X1 has an address part (operand reference) X2. The operand needed to execute the instruction is stored in the memory word with address X3.An index register contains the value X4.What is the relationship between these various quantities if the addressing mode of the instruction is: (10 marks)

(i) Direct;
(ii) Indirect;
(iii) Displacement;
(iv) Indexed;
(v) Immediate ;

QUESTION FIVE (20 MARKS)

(i.a) Discuss the following memory access modes. Give the memory devices involved in each case.
(6 marks)

(i) Random Access
(ii) Sequential Access
(iii) Direct Access

(i.b) A cache may be organized such that:
- In one case, there are more data elements per block and fewer blocks
- In another case, there are fewer elements per block but more blocks

However, in both cases – i.e. larger blocks but fewer of them OR shorter blocks, but more of them – the cache's total capacity (amount of data storage) remains the same. What are the merits and demerits of each organization? Support your answer with a short example assuming that the cache is direct mapped. (6 marks)

(i.c) Briefly discuss the Flynn's classification of computer systems processors. (8 marks)
