CHUKA UNIVERSITY

UNIVERSITY EXAMINATIONS

EXAMINATION FOR THE AWARD OF DEGREE OF BACHELOR OF SCIENCE IN COMPUTER SCIENCE

COSC 110: COMPUTER ARCHITECTURE

STREAMS: BSC (COMPUTER SCIENCE) Y1S1 **TIME: 2 HOURS**

DAY/DATE: MONDAY 03/12/2018 **2.30 P.M. – 4.30 P.M.**

INSTRUCTIONS:

- **Answer question One and any other two questions**

Question One (30 marks)

(a) State the role of the following registers in instruction execution.

(i) Program Counter (1 mark)

(ii) Instruction Register (1 mark)

(b) Using a diagram, outline the four basic parts of a computer as outlined by the von Neumann architecture. (4 marks)

(c) Explain difference between write-through and write-back cache write policies. (4 marks)

(i) write-through

(ii) write-back

(d) Interrupts are said to provide efficiency in tasks processing. In light of instruction execution, justify this statement. (4 marks)

(e) In the event that interrupts are enabled, explain how the flow of program execution is affected. (4 marks)

(f) Explain the differences between two-address and three-address instruction sets in processor architecture. Give an example to illustrate your answers. (4 marks)

(g) Given an expression `x = y * z + q`

(i) Represent the instructions using stack architecture. (4 marks)

(ii) Represent the instructions using two address general purpose register. Use two registers R1 and R2. (4 marks)

Question Two (20 marks)

(a) Discuss the difference between little endian and big endian byte ordering. Use an example of the word 12345678 to illustrate your discussion. (6 marks)

(b) Discuss three differences between Dynamic RAM and Static RAM. (6 marks)

(c) Given an instruction `ADD R1, R2`

(i) Explain the addressing scheme used in the instruction. (2 marks)

(ii) In the processor architecture, which registers could represent R1 and R2 and why? (3 marks)

(iii) Explain the expected interpretation and execution of the instruction.(3 marks)

Question Three (20 marks)

(a) A cache may be organized such that:

- In one case, there are more data elements per block and fewer blocks
- In another case, there are fewer elements per block but more blocks

However, in both cases i.e. larger blocks but fewer of them OR shorter blocks, but more of them, the cache's total capacity (amount of data storage) remains the same.
What are the pros and cons of each organization? Support your answer with a short example assuming that the cache is direct mapped. (6 marks)

(b) The 5 stages of the processor have the following latencies:

	Fetch	Decode	Execute	Memory	Write back
Ia	200ps	300ps	200ps	400ps	100ps

Assume that when pipelining, each pipeline stage costs 10ps extra for the registers between pipeline stages.

(i) For a pipelined processor, what is the cycle time? What is the latency of an instruction? What is the throughput? (3 marks)

(ii) For a non-pipelined processor, explain the difference in cycle time, latency, and throughput if any. (3 marks)

(c) Using an illustration of three instructions I_1, I_2, and I_3 discuss the concept of pipelining in the design of computer systems. Show the arrangement of the IF, ID, IE, MEM, and WB phases in each instruction cycle. (8 marks)

Question Four (20 marks)

(a) Given a memory reference a Cache has to determine if the memory is in the Cache. There are a number of schemes for determining where a global memory reference should be placed in the cache memory. Describe the following Schemes: Direct mapped and n-way associative mapping caches. (6 points)

(b) Discuss the following memory access modes. Give the memory devices involved in each case. (6 marks)

(i) Direct access
(ii) Sequential access
(iii) Random access

(c) Consider a *8-way set-associative* cache
- Data words are *32 bits* long
- Words are addressed to the *half-word*
- The cache holds 2 Mbytes of data
- Each block holds 16 data words
- Physical addresses are 32 bits long

How many bits of tag, index (set), and offset (word address) are needed to support references to this cache? (8 marks)

Question Five (20 marks)

(a) Discuss the operation of Interrupt Driven I/O in view of:
(i) The I/O Module (4 marks)
(ii) The processor (4 marks)
(iii) List two advantages of this approach compared to Programmed I/O. (4 marks)

(b) Discuss the operation of the cache as used by the processor citing the role of RAM in this operation. (8 marks)
